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TITLE: Method and structure for testing embedded cores based system-on-a-chip

DATE-ISSUED: June 19, 2001

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U.S. PATENT DOCUMENTS

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
5535164	July 1996	Adams et al.	N/A
5617531	April 1997	Crouch et al.	N/A
5619512	April 1997	Kawashima et al.	N/A
5748640	May 1998	Jiang et al.	714/720
5825785	October 1998	Barry et al.	714/732
5954824	September 1999	Cherichetti et al.	714/28
5963566	October 1999	Rajsuman et al.	714/733
5991898	November 1999	Rajski et al.	714/30
6003142	December 1999	Mori	714/30

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ABSTRACT:

A method of testing embedded cores in an integrated circuit chip having a microprocessor core, a memory core and other functional cores therein. The method includes the steps of; forming a plurality of registers in the integrated circuit chip, testing the microprocessor core by executing its instructions multiple times with pseudo random data and evaluating the results by comparing simulation results, applying a test program to the microprocessor core to generate a memory test pattern by the microprocessor core, applying the memory test pattern to the memory core by the microprocessor core and evaluating the response of the memory core by the microprocessor core, and testing the other functional cores by applying a function specific test pattern thereto by the microprocessor core and evaluating the resultant output signals of the functional cores.

17 Claims, 16 Drawing figures

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